

IN THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. – 13. (canceled)

14. (original) A silicon-on-insulator structure comprising:

a body layer comprising source, drain, and channel regions, the channel region being positioned between the source and drain regions;

a highly-doped substrate layer, the highly-doped substrate layer being doped to a first doping polarity;

an insulator layer between the body layer and the highly-doped substrate layer;

wherein the highly-doped substrate layer comprises two compensated regions adjacent the insulator layer and aligned with the source and drain regions, and an uncompensated region between the two compensated regions aligned with the channel region, the compensated regions being further doped with dopants of a second polarity opposite the first polarity.

15. (original) The silicon-on-insulator structure of claim 14 wherein the source and drain regions are doped to a second doping polarity.

16. (original) The silicon-on-insulator structure of claim 15 wherein the channel region is doped to the first doping polarity.

17. (original) The silicon-on-insulator structure of claim 14 wherein the compensated regions are doped with dopants of a second polarity to a concentration substantially

equivalent to the concentration of the first doping polarity of the uncompensated region.

18. (original) The silicon-on-insulator structure of claim 14 further comprising a masking structure to substantially shield the channel region from implantation of dopants of a second polarity into the compensated regions.
19. (original) The silicon-on-insulator structure of claim 18 wherein the masking structure comprises a gate.
20. (original) The silicon-on-insulator structure of claim 16 wherein the second polarity is an N-type polarity and the first polarity is a P-type polarity, forming a NMOS structure.
21. (original) The silicon-on-insulator structure of claim 16 wherein the second polarity is an P-type polarity and the first polarity is a N-type polarity, forming a PMOS structure.
22. (original) The silicon-on-insulator structure of claim 16 wherein the thin substrate layer and highly-doped substrate layer comprise silicon, and wherein the insulator layer comprises silicon dioxide.
23. (original) The method of claim 22 wherein the body layer and insulator layer both have a thickness of about 100 angstroms, the uncompensated and channel region are doped

to a first doping polarity at a concentration of about  $1 \times 10^{19}$  first dopant atoms per cubic centimeter, the source and drain regions are doped to a second doping polarity at a concentration of about  $1 \times 10^{21}$  second dopant atoms per cubic centimeter, and wherein the compensated regions are doped to a second doping polarity at a concentration of about  $1 \times 10^{19}$  second dopant atoms per cubic centimeter.

24. (original) The method of claim 23 wherein the first dopant atoms are boron atoms, and wherein the second dopant atoms are selected from the group consisting of arsenic and phosphorus atoms.
25. (original) The method of claim 23 wherein the second dopant atoms are boron atoms, and wherein the first dopant atoms are selected from the group consisting of arsenic and phosphorus atoms.

Respectfully submitted,

Date: 8/2/05



Michael D. Plimier  
Reg. No. 43,004  
ATTORNEY FOR APPLICANTS

Intel Corporation  
Mail Stop SC4-202  
P.O. Box 5326  
Santa Clara, CA 95056-5326  
(408) 765-7857

-6-

Serial No.: 10/806,609

Attorney Docket: P14691D

**CERTIFICATE OF TRANSMISSION**  
(37 C.F.R. § 1.8(a))

I hereby certify that this correspondence is being transmitted by facsimile to the United States Patent and Trademark Office on Aug. 2, 2005.

Michael Plimier  
Name of Person Sending Facsimile

  
\_\_\_\_\_  
Signature

-7-

Serial No.: 10/806,609

Attorney Docket: P14691D